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EXAMINER	
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2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/593,549	BRESSY ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 September 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *45-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *45-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/19/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

I. ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

1. As required by **M.P.E.P. 609(C)**, the applicant's submissions of the Information Disclosure Statement dated September 19, 2006 is acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by **M.P.E.P 609 C(2)**, a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

II. OBJECTIONS TO THE ABSTRACT

2. Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because form and legal phraseology often used in patent claims are utilized in constructing the abstract; preferably, the abstract should provide brief disclosure to assist reader gaining a general understanding of the invention and decide whether there is a need for consulting the full patent text for detail. Correction is required. See MPEP § 608.01(b).

III. OBJECTIONS TO THE SPECIFICATION

5. The disclosure is objected to because of the following informalities: Multiple instances through out the Specification have following misspelled words: "authorising," “authorisation,” “authorise,” “initialised,” “initialisation” and “unauthorised.”

Appropriate correction is required.

IV. OBJECTIONS TO THE CLAIMS

6. Claims 45, 47, 49, 51, 57, 61, 63, 69 and 70 are objected to because of the following informalities associated with misspelling.

As per claims 45, 49, 51, 57, 61, 69 and 70, multiple instances with regard to the misspelling of "authorisation," which should be replaced with “authorization.”

As per claims 63 and 70, with regard to the misspelling of "initialised," which should be replaced with “initialized.”

As per claims 63 and 70, multiple instances with regard to the misspelling of "initialising," which should be replaced with “initializing.”

As per claims 57 and 69, claims 57 and 69 appear to be independent claims, but each claim include the claimed limitation referencing to the independent claim 45, thus claims 57 and 69 appear to be dependent claims of independent claim 45; the examiner will assume claims 57 and 69 as independent claims, without having claims 57 and 69 referencing to independent claim 45, for the current examination.

As per claim 47, in line 1, “Control hardware …” should be replaced with -Access control hardware …-.

As per claim 70, in line 3, “consists in” should be replaced with -consist of-.

Appropriate correction is required.

V. REJECTIONS BASED ON 35 U.S.C. 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claims 45, 47-49, 52-53, 56-57, 60-61, 63-66 and 68-73 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 45 recites the limitation "said reference value" in line 11. There is insufficient antecedent basis for this limitation in the claim.

Claim 47 recites the limitation "(NMI1)" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 47 recites the limitation "said interrupt" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 48 recites the limitation "(NMI1)" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 49 recites the limitation "said trigger code (Code-DD)" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 52 recites the limitation "said validation signal" in lines 4 and 6-7. There is insufficient antecedent basis for this limitation in the claim.

Claim 52 recites the limitation "said access request electrical signal" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 53 recites the limitation "said access validation electrical signal" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 56 recites the limitation "said access validation electrical signal" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 56 recites the limitation "said access code" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 57 recites the limitation "said comparison step (E30)" in line 9. There is insufficient antecedent basis for this limitation in the claim.

Claim 57 recites the limitation "said reference value" in line 11. There is insufficient antecedent basis for this limitation in the claim.

Claim 61 recites the limitation "said trigger code (Code-DD)" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 64 recites the limitation "the validation signal" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim 64 recites the limitation "said access electrical signal" in line 6. There is insufficient antecedent basis for this limitation in the claim.

Claim 64 recites the limitation "said access request electrical signal" in line 7. There is insufficient antecedent basis for this limitation in the claim.

Claim 65 recites the limitation "said access validation electrical signal" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 68 recites the limitation "said trigger code (Code-DD)" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 72 recites the limitation "said access instruction" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claim 73 recites the limitation "said predetermined law" in line 2. There is insufficient antecedent basis for this limitation in the claim.

As per claim 45, in line 8, the use of the claimed limitation of "… so-called validation means …" is vague as to exactly what the applicant is claiming; the examiner will assume the claimed limitation of "... validation means designed to generate …" for the current examination .

As per claim 45, in line 10, it is not fully clear if "processor" is a different/same processor as previously recited; the examiner will assume the claimed limitation of "… the processor …" for the current examination.

As per claim 45, in line 11, it is not fully clear which of "said reference value" the applicant is referring to; the examiner will assume the claimed limitation of "… said predetermined reference value …" for the current examination.

As per claims 47 and 48, in line 1, it is not fully clear which "it" the applicant is referring to; the examiner will assume the following claimed limitation of "… wherein said hardware unit additionally includes ..." for the current examination.

As per claim 47, in line 3, it is not fully clear which "(NMI1)" the applicant is referring to; the examiner will assume the claimed limitation of "… said control interrupt is designed …" for the current examination.

As per claim 47, in line 3, it is not fully clear which "said interrupt" the applicant is referring to; the examiner will assume the claimed limitation of "… said control interrupt is designed to follow the acquisition of said trigger code …" for the current examination.

As per claim 48, in line 4, it is not fully clear which "(NMI1)" the applicant is referring to; the examiner will assume the claimed limitation of "… said control interrupt depending on the outcome …" for the current examination.

As per claim 49, in line 1, it is not fully clear which "it" the applicant is referring to; the examiner will assume the following claimed limitation of "… wherein said hardware unit includes ..." for the current examination.

As per claim 49, in line 3, it is not fully clear which "said trigger code (Code-DD)" the applicant is referring to; the examiner will assume the claimed limitation of "… said access authorization code (Code-AA) is different …" for the current examination.

As per claim 52, in lines 4 and 6-7, it is not fully clear which "said validation signal" the applicant is referring to; the examiner will assume the claimed limitation of "… generate an validation signal to validate …" (in claim 45, lines 8-9) for the current examination.

As per claim 52, in line 6, it is not fully clear which "said access request electrical signal " the applicant is referring to; the examiner will assume the claimed limitation of "… receive an access request electrical signal requesting access (CS-RQ, WE-RQ) to said peripheral (P) …" (in claim 52, line 3) for the current examination.

As per claim 53, in line 4, it is not fully clear as to which of "this state" the applicant is referring to; the examiner will assume the claimed limitation of "... as a function of the state (RQ_0, RQ_1) of said access request electrical signal …" for the current examination.

As per claim 53, in line 5, it is not fully clear as to which of "… said access validation electrical signal …" the applicant is referring to; the examiner will assume the claimed limitation of "… said validation signal …" for the current examination.

As per claim 56, in lines 3-4, it is not fully clear as to which of "said access validation electrical signal" and "said access code" the applicant is referring to; the examiner will assume the claimed limitation of "... generation of said validation signal (SIG_VAL), or from the acquisition of said access authorization code …" for the current examination.

As per claim 57, in line 2, it is not fully clear which "it" the applicant is referring to; the examiner will assume the following claimed limitation of "… wherein said method includes ..." for the current examination.

As per claim 57, in line 9, it is not fully clear which of "said comparison step (E30)" the applicant is referring to; the examiner will assume the claimed limitation of "… said comparison step ..." for the current examination.

As per claim 57, in line 11, it is not fully clear which of "said reference value" the applicant is referring to; the examiner will assume the claimed limitation of "… said predetermined reference value …" for the current examination.

As per claim 60, in line 1, it is not fully clear which "it" the applicant is referring to; the examiner will assume the claimed limitation of "… wherein said method additionally includes…" for the current examination.

As per claim 61, in line 1, it is not fully clear which "it" the applicant is referring to; the examiner will assume the claimed limitation of "… wherein said method includes…" for the current examination.

As per claim 61, in line 3, it is not fully clear which "said trigger code (Code-DD)" the applicant is referring to; the examiner will assume the claimed limitation of "… said access authorization code (Code-AA) is different …" for the current examination.

As per claim 63, in line 2, it is not fully clear which "it" the applicant is referring to; the examiner will assume the claimed limitation of "… said method additionally includes…" for the current examination.

As per claim 63, in line 3, it is not fully clear which of "said generation step" the applicant is referring to; the examiner will assume the claimed limitation of "… said generation of said predetermined reference value …" for the current examination.

As per claim 64, in line 2, it is not fully clear as to which "validation signal" the applicant is referring to; the examiner will assume the clamed limitation of "… generation (E50) a validation signal ..." (in claim 57, line 8) for the current examination.

As per claim 64, in line 6, it is not fully clear which "said access electrical signal " the applicant is referring to; the examiner will assume the claimed limitation of "… said access signal …" for the current examination.

As per claim 64, in line 7, it is not fully clear which "said access request electrical signal " the applicant is referring to; the examiner will assume the claimed limitation of "… the state (RQ_0, RQ_1) of an access request electrical signal (CS-RQ, WE-RQ)

requesting access to said peripheral (P) is read …" (in claim 64, lines 3-4) for the current examination.

As per claim 65, it is not fully clear as to how the interrupted is maskable and at the same time non-maskable; the examiner will assume the claimed limitation of "... triggering a interrupt of said processor, termed an alarm interrupt, preferably non-maskable (NMI2) …" for the current examination.

As per claim 65, in line 4, it is not fully clear as to which "said state" the applicant is referring to; the examiner will assume the claimed limitation of "…a function of said state (RQ_0, RQ_1) of said access request electrical signal …" for the current examination.

As per claim 65, in line 5, it is not fully clear as to which "said access validation electrical signal" the applicant is referring to; the examiner will assume the claimed limitation of "… said validation signal (SIG_VAL) …" for the current examination.

As per claim 66, in line 1, it is not fully clear which "it" the applicant is referring to; the examiner will assume the claimed limitation of "… said method includes …" for the current examination.

As per claim 68, in line 3, it is not fully clear which of "said trigger code" the applicant is referring to; the examiner will assume the claimed limitation of "… after a predetermined delay counted from said step (E50) of generating the validation signal (SIG_VAL) …" for the current examination.

As per claim 69, in line 1, it is not fully clear which "it" the applicant is referring to; the examiner will assume the claimed limitation of "… said method includes …" for the current examination.

As per claim 69, in line 6, it is not fully clear if the “access authorization coded” is the same/different access authorization code previously recited; the examiner will assume the claimed limitation of "... a step (E520) of sending the access authorization code (Code-AA) …” for the current examination.

As per claim 70, in line 2, it is not fully clear which "it" the applicant is referring to; the examiner will assume the claimed limitation of "… said method additionally includes …" for the current examination.

As per claim 70, in line 4, it is not fully clear which of "this code" the applicant is referring to; the examiner will assume the claimed limitation of "… before each sending (S100) of said access authorization code (Code-AA) to said hardware unit …" for the current examination.

As per claim 71, in line 1, it is not fully clear which "it" the applicant is referring to; the examiner will assume the claimed limitation of "… said method additionally includes …" for the current examination.

As per claim 71, in line 2, it is not fully clear which of "… said alarm routine …" the applicant is referring to; the examiner will assume the claimed limitation of "… said alarm interrupt routine including a step of generating …" for the current examination.

As per claim 71, in line 3, it is not fully clear if the claimed limitation should be “and” or “or”; the examiner will assume the claimed limitation of "… or …" for the current examination.

As per claim 72, in line 2, it is not fully clear which "it" the applicant is referring to; the examiner will assume the claimed limitation of "… wherein said computer program includes an instruction (E620) …" for the current examination.

As per claim 72, in lines 3-4, it is not fully clear which of "… said access instruction …" the applicant is referring to; the examiner will assume the claimed limitation of "… Computer program including an access instruction …" (in claim 72, line 1) for the current examination.

As per claim 73, in line 1, it is not fully clear which "it" the applicant is referring to; the examiner will assume the claimed limitation of "… wherein said computer program additionally includes means of generating …" for the current examination.

As per claim 73, in line 2, it is not fully clear which of "… said predetermined law …" the applicant is referring to; the examiner will assume the claimed limitation of "… a predetermined law …” for the current examination.

VI. REJECTIONS BASED ON 35 U.S.C. 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 72-73 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. As "computer program" having instructions are considered non-statutory subject matter. Please see MPEP 2106.01.

VII. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 45-50, 52-55, 57-62, 64-67, 69 and 71-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayan et al. (US Patent 6,711,690) in view of Albrecht (US Patent 6,510,521).

10. As per claims 45 and 57, Dayan teaches a hardware unit (Fig. 1, ref. 190) executing a method for controlling access, by a processor (Fig. 1, ref. 130) to a peripheral (P) (Fig. 1, ref. 170) of this processor, said hardware unit executing said method including:

means of triggering (E34) an interrupt of said processor, termed a control interrupt (Fig. 2 and col. 3, l. 39 to col. 4, l. 66), as the interrupt is trigger in response to an unblock request;

means of obtaining, after said triggering, an authorization code to said peripheral (P) (col. 4, ll. 23-49 and col. 5, ll. 20-46), as the authorization code is obtained for verification;

validating of said authorization code to ensure that the unblock request is authorized (Fig 3-4 and col. 4, l. 23 to col. 5, l. 46); and

validation means designed to generate (E50) a validation signal (SIG_VAL) (e.g. block signal) to validate an access electrical signal (access signal) (CS, WE, PWR) (e.g. unblock write enable signal) to said peripheral (P), depending on the outcome of said validating of said authorization code, wherein said hardware unit (Fig. 1, ref. 190) is external to the processor (Fig. 1, ref. 130) (Fig 2-4 and col. 3, l. 39 to col. 5, l. 46).

Dayan does not expressly teach said hardware unit executing said method including: means of obtaining (E37), from said processor, an access authorization code (Code-AA); internal means of comparing said access authorization code with a predetermined reference value; and means of generating said predetermined reference value according to a predetermined law.

Albrecht teaches an authentication method including:

means of obtaining, from a processor (Fig. 3, ref. 212), an access authorization code (Fig. 2, ref. 114) (Fig. 1-3 and col. 2, l. 46 to col. 4, l. 45), as the processor respond and process the SMI for implementing the authenticating function and provides the access authorization code to be authenticated;

internal means of comparing (Fig. 2, ref. 120) said access authorization code (Fig. 2, ref. 114) with a predetermined reference value (Fig. 2, ref. 102, 104, 116); and

means of generating said predetermined reference value (e.g. electronic signature) according to a predetermined law (e.g. predetermined manner) (Fig. 1-2 and col. 1, ll. 36-44) as the electronic signature is generated in the predetermined manner.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Albrecht's authentication method into Dayan's hardware unit for the benefit of implementing a more robust approach to preventing unauthorized access to the peripheral (Albrecht, col. 1, ll. 27-28) to obtain the invention as specified in claims 45 and 57.

11. As per claim 69, Dayan teaches a method of managing access to a peripheral (P) (Fig. 1, ref. 170), wherein said method includes a step of implementing a routine (IRT1) associated with a control interrupt, preferably non-maskable (NMI1) (Fig. 2 and col. 3, l. 39 to col. 5, l. 5), said control routine including:

a step of receiving an unblock request for accessing said peripheral (col. 3, l. 39 to col. 5, l. 9); and

a step (E520) of sending an authorization code to an access control hardware unit (Fig. 1, ref. 190) (Fig 2-4 and col. 3, l. 39 to col. 5, l. 46), as the authorization code is included in the unblock request.

Dayan does not teach the method comprising a step (E510) of generating, according to a predetermined law, an access authorization code.

Albrecht teaches an authentication method including generating an access authorization code (Fig. 2, ref. 114) according to a predetermined law (Fig. 1-2; col. 1, ll.

36-44 and col. 2, l. 46 to col. 3, l. 47), as the generation of the access authorization code need to be implemented in a predetermined manner in order to properly determine if authorization may be granted.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Albrecht's authentication method into Dayan's hardware unit for the benefit of implementing a more robust approach to preventing unauthorized access to the peripheral (Albrecht, col. 1, ll. 27-28) to obtain the invention as specified in claim 69.

12. As per claims 46 and 58, Dayan and Albrecht teach all the limitations of claims 45 and 57 as discussed above, where Dayan further teaches the access control hardware unit executing the method comprising wherein said control interrupt is a non-maskable interrupt (NMI1) (Dayan col. 3, ll. 39-58).

13. As per claims 47 and 59, Dayan and Albrecht teach all the limitations of claims 45 and 57 as discussed above, where Dayan further teaches the access control hardware unit executing the method comprising wherein said hardware unit additionally includes means of obtaining a trigger code (Code-DD) (e.g. unblock request), and in that said means of triggering said control interrupt is (triggering step (E34)) designed to follow the acquisition of said trigger code (Code-DD) (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5).

14. As per claims 48 and 60, Dayan and Albrecht teach all the limitations of claims 47 and 59 as discussed above, where both further teach the access control hardware unit executing the method comprising wherein said hardware unit additionally includes means of comparing said trigger code (Code-DD) with said predetermined reference value (Code-UMCA), and in that said triggering means are designed to trigger said control interrupt depending on the outcome of said comparison (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5 and Albrecht, Fig. 1-2 and col. 2, l. 46 to col. 3, l. 47), as the unblock request is authorized via the comparison of the digests.

15. As per claims 49 and 61, Dayan and Albrecht teach all the limitations of claims 45 and 57 as discussed above, where Dayan further teaches the access control hardware unit executing the method comprising wherein said hardware unit includes means of triggering an interrupt of said processor, termed an alarm interrupt, when said access authorization code (Code-AA) is different from the predetermined reference value (Code-UMCA) (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5), as the unblock request failed authorization and the incident is reported via the alarm interrupt.

16. As per claims 50 and 62, Dayan and Albrecht teach all the limitations of claims 49 and 61 as discussed above, where Dayan further teaches the access control hardware unit executing the method comprising wherein said alarm interrupt is a non-maskable interrupt (NMI2) (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5).

17. As per claims 52 and 64, Dayan and Albrecht teach all the limitations of claims 45 and 57 as discussed above, where Dayan further teaches the access control hardware unit executing the method comprising wherein said validation means include logic combination means designed to:

receive and read an access request electrical signal (Dayan, write enable of Fig. 2) requesting access (CS-RQ, WE-RQ) (Fig. to said peripheral (P) (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5), as the access request electrical signal is received and read by the logic circuit (Dayan, Fig. 2, ref. 250);

receive and read said validation signal (SIG_VAL) (Dayan, block signal of Fig. 2) (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5), as the validation signal is received and read by the logic circuit (Dayan, Fig. 2, ref. 250); and

validate said access electrical signal (access signal) (CS, WE) as a function of a state (RQ_0, RQ_1) of said access request electrical signal (CS-RQ, WE-RQ), a state (VAL_0, VAL_1) of said validation signal, and a logic represented in a truth table (function of a logic rule) (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5), as the logical representation associated with the logic circuit (Dayan, Fig. 2, ref. 250) validates the access electrical signal in accordance to the state of the received signals .

18. As per claims 53 and 65, Dayan and Albrecht teach all the limitations of claims 52 and 64 as discussed above, where Dayan further teaches the access control hardware unit executing the method comprising means of reading a state (RQ_0, RQ_1) of said access request electrical signal (CS_RQ, WE_RQ), and means of

triggering an interrupt of said processor, termed an alarm interrupt (NMI2), preferably non-maskable, as a function of the state (RQ_0, RQ_1) of said access request electrical signal and of said state (VAL_0, VAL_1) of said validation signal (SIG_VAL) (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5), as the access is unauthorized and the incident is reported via the alarm interrupt.

19. As per claims 54 and 66, Dayan and Albrecht teach all the limitations of claims 45 and 57 as discussed above, where Dayan further teaches the access control hardware unit executing the method comprising wherein it includes means of inhibiting said validation signal (SIG_VAL) (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5), as the write access is inhibited by re-blocking the write access.

20. As per claims 55 and 67, Dayan and Albrecht teach all the limitations of claims 54 and 66 as discussed above, where Dayan further teaches the access control hardware unit executing the method comprising wherein said inhibiting means are designed to inhibit said validation signal (SIG_VAL) following at least one access to said peripheral (P) (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5), as the write access is inhibited by re-blocking the write access after at least one access to the peripheral.

21. As per claim 71, Dayan and Albrecht teach all the limitations of claim 69 as discussed above, where Dayan further teaches the method comprising wherein said method additionally includes a step of implementing an alarm interrupt routine (IRT2),

said alarm interrupt routine including a step of generating an alert or inhibiting the use of said peripheral (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5), wherein the alert is generated via reporting the unauthorized accessing.

22. As per claim 72, Dayan and Albrecht teach all the limitations of claim 45 as discussed above, where Dayan further teaches a computer program including an access instruction (E630) to access a peripheral (P), wherein said computer program includes an instruction (E620) to send a trigger code (Code-DD) to an access control hardware unit of said peripheral (P) according to claim 45, before the execution of said access instruction (Dayan, col. 6, ll. 14-39), as the hardware unit disclosed in claim 45 is able to be implemented in form of computer-readable instructions.

23. As per claim 73, Dayan and Albrecht teach all the limitations of claim 72 as discussed above, where both further teach the computer program comprising wherein said computer program additionally includes means of generating said trigger code (Code-DD) according to a predetermined law (e.g. predetermined manner) (Dayan, Fig. 2-4; col. 3, l. 39 to col. 5, l. 5 and Albrecht, Fig. 1-2; col. 1, ll. 36-44; col. 2, l. 46 to col. 4, l. 45).

24. As per claim 74, Dayan and Albrecht teach all the limitations of claim 69 as discussed above, where Dayan further teaches a processor designed to implement a method of managing access according to claim 69 (Dayan, col. 6, ll. 14-39).

25. As per claim 75, Dayan and Albrecht teach all the limitations of claim 45 as discussed above, where both further teach the use of an access control hardware unit (20) according to claim 45, to validate an access signal to a peripheral (P) which can in particular be selected from a screen, a keyboard, a memory, a communications interface controller, a memory management unit (MMU) or a memory protection unit (MPU) (Dayan, Fig. 1-4; col. 3, l. 39 to col. 5, l. 5 and Albrecht, Fig. 1-3; col. 2, l. 46 to col. 4, l. 45).

26. As per claim 76, Dayan and Albrecht teach all the limitations of claim 72 as discussed above, where Dayan further teaches a processor designed to implement a computer program 72 according to claim 72 (Dayan, col. 6, ll. 14-39).

27. Claims 51, 63 and 70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayan et al. (US Patent 6,711,690) in view of Albrecht (US Patent 6,510,521) as applied to claims 45, 57 and 69 above, and further in view of Cardillo et al. (US Patent 5,928,362).

28. As per claims 51 and 63, Dayan and Albrecht teach all the limitations of claims 45 and 57 as discussed above, where both further teach the access control hardware unit executing the method comprising initializing said predetermined reference value (Code-UMCA) in said hardware unit when switch on, and in that, according to said

predetermined law, authenticating each time said access authorization code (Code-AA) is obtained and said predetermined reference value is generated (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 46 and Albrecht, Fig. 1-2; col. 2, l. 46 to col. 3, l. 47 and col. 4, l. 56 to col. 5, l. 26).

Dayan and Albrecht do not teach a counter, and said counter is incrementing during authentication.

Cardillo teach an access authentication method comprising a counter (Fig. 4, ref. 418) and said counter is incrementing during authentication (col. 8, l. 16 to col. 9, l. 11), as the address counter is incremented during authentication for accessing.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Cardillo's counter into Dayan and Albrecht's hardware unit for the benefit of enabling authentication checking while minimizing the physical and electrical differences with prior art standards (Cardillo, col. 4, ll. 19-21) to obtain the invention as specified in claims 51 and 63.

29. As per claim 70, Dayan and Albrecht teach all the limitations of claim 69 as discussed above, where both further teach the method comprising initializing said access authorization code (Code-AA), and in that said generation step (E510) consists of authenticating (e.g. authenticating the unblock request) before each sending (S100) of said access authorization code (Code-AA) to said hardware unit (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 46 and Albrecht, Fig. 1-2; col. 2, l. 46 to col. 3, l. 47 and col. 4, l. 56 to col. 5, l. 26).

Dayan and Albrecht do not teach a counter, and said counter is incrementing during authentication.

Cardillo teach an access authentication method comprising a counter (Fig. 4, ref. 418) and said counter is incrementing during authentication (col. 8, l. 16 to col. 9, l. 11), as the address counter is incremented during authentication for accessing.

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Cardillo's counter into Dayan and Albrecht's hardware unit for the benefit of enabling authentication checking while minimizing the physical and electrical differences with prior art standards (Cardillo, col. 4, ll. 19-21) to obtain the invention as specified in claim 70.

30. Claims 56 and 68 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dayan et al. (US Patent 6,711,690) in view of Albrecht (US Patent 6,510,521) as applied to claims 54 and 66 above, and further in view of Zinsky et al. (US Patent 6,480,097).

Dayan and Albrecht teach all the limitations of claims 54 and 66 as discussed above, where Dayan further teaches the access control hardware unit executing the method comprising wherein said inhibiting means are designed to inhibit said validation signal (SIG_VAL) after the generation of said validation signal (SIG_VAL), or from the acquisition of said access authorization code (Code-AA) (Dayan, Fig. 2-4 and col. 3, l. 39 to col. 5, l. 5), as the write access is inhibited by re-blocking the write access after accessing the peripheral.

Dayan and Albrecht do not teach the access control hardware unit executing the method comprising a predetermined delay after access is granted.

Zinsky teaches au authorization method comprising a predetermined delay (Fig. 3, ref. 446) after access is granted (Fig. 3, ref. 442) (col. 8, ll. 36-58).

It would have been obvious for one of ordinary skill in this art, at the time of invention was made to include Zinsky's delay into Dayan and Albrecht's hardware unit for the benefit of enhancing the security of the hardware unit (Zinsky, col. 2, ll. 13-25) to obtain the invention as specified in claims 56 and 68.

VIII. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 45-76 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

February 19, 2008

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